Amendment to the Claims

Please amend the claims in the manner indicated.

1. (currently amended) A method for storing data in a cache comprising:
prioritizing a locked way of the cache higher than a recently used way; [[and]]
prioritizing an additional locked way higher than the locked way;
setting a first bit to indicate priority of the locked way;
setting a second bit to indicate priority of the additional locked way; and
setting a third bit to indicate priority of a recently used way.

2. (original) The method of claim 1, further comprising storing data in the recently used way.

3. (original) The method of claim 1, further comprising:
prioritizing the locked way higher than a least recently used way; and
storing data in the least recently used way.

4. (original) The method of claim 1, further comprising locking at least one way of the cache to provide the locked way.

5. (original) The method of claim 1, further comprising reading data from a way of the cache prior to prioritizing the locked way, the way being the recently used way.

6. (original) The method of claim 1, wherein prioritizing the locked way includes setting a bit in a register.

7. (original) The method of claim 1, further comprising setting a bit in a register to indicate priority of the recently used way.

8. (original) The method of claim 1, further comprising writing data to a way of the cache prior to prioritizing the locked way, the way being the recently used way.

9-12. (cancelled)

13. (currently amended) A method comprising:

locking a first way of a cache;

locking a second way of the cache;

accessing a third way of the cache; and

using a first bit to prioritize the first way, a second bit to prioritize the second way higher than the first way, and a third bit to prioritize a recently used way.

~~prioritizing the first way of the cache higher than the second way of the cache.~~

14. (currently amended) The method of claim 13, wherein locking the first way includes setting [[a]] the first bit in a register to indicate the priority of the first way.

15-16. (cancelled)

17. (currently amended) An apparatus comprising a cache having a first way and a second way, the apparatus further comprising:

a circuit adapted to lock the first way and the second way and to prioritize the first locked way higher than the second locked way, the circuit further adapted to use a first bit to indicate priority of the first way, a second bit to indicate priority of the second way, and a third bit to indicate priority of a recently used way.

18. (cancelled)

19. (previously presented) The apparatus of claim 17, further comprising a memory location adapted to indicate the priorities of the first way and the second way.

20-22. (cancelled)